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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/651,874	08/29/2003	Leonard O. Farnsworth III	BUR920030103US1	9345

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EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/651,874	FARNSWORTH ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

GUY LAMARRE
PRIMARY EXAMINER

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are currently pending and have examined.

Drawings

2. Figure 6 is objected to because in box 295 the word "limited" should be changed to "limit". Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: Page 6, l. 12, "NPG circuit scan chains by a bus 175" should be "NPG circuit scan chains 170 by a bus 175".

Appropriate correction is required.

Claim Objections

4. Claims 1-20 are objected to because of the following informalities: the phrase "macro circuit" is missing a hyphen and should be written, "macro-circuit" for consistency. Applicants are responsible for checking all claims to assure this is corrected. Appropriate correction is required.

5. Claim 13 is objected to because the phrase "a predetermined number" should be changed to "a predetermined limit" to correspond to the specification/.

6. Claims 3, 5 and 6 is objected to because in the phrase "adapted to" the claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed, or by claim language that does not limit a claim to a particular structure. See MPEP 2111.04. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3, 5, 6, 9-12, 14, 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Shubat et al. (US-6363020), hereinafter Shubat.

Claim 1:

Shubat teaches a multiplicity of macro-circuits (**memory instances 204A – 204D, Fig. 3A**), each macro circuit having the same function, a fuse bank (**Fuses Box 206, Fig. 3A**) containing a multiplicity of fuses, the state of said fuses storing test data indicating at least which macro-circuits failed a test, and means for preventing utilization of failing macro-circuits during operation of said integrated circuit (**registers 208A through 208D, Fig. 3A**). (Abstract, Col. 2, l. 46 to col. 3, l. 37, col. 7, l. 47 to col. 8, l. 20, claim 1).

Claim 2:

Shubat teaches means for isolating inputs and outputs of said macro-circuit during testing of said macro-circuits and during testing of additional circuits of said integrated circuit in that The contents of the individual registers 208A-208D are then used for effectuating row redundancy (wordline replacement) or column redundancy (bitline replacement wherein a redundant block of bitlines are selected and a faulty block of primary memory bitlines are de-selected) in a particular memory instance. (Abstract, Col. 2, l. 46 to col. 3, l. 37, col. 7, l. 47 to col. 8, l. 20, col. 13, ll. 18-44, claim 1).

Claim 3:

Shubat teaches including isolation circuits adapted to, during testing of said macro-circuits, isolate each macro-circuit from additional circuits of said integrated circuit and couple a single macro-circuit into a single scan chain (**registers 208A through 208D, Fig. 3A**), the output of said single scan chain observable at an I/O pad of said integrated circuit (**via RSCOUT, Figs. 5A and 5B**). (Abstract, Col. 2, l. 46 to col. 3, l. 37, col. 7, l. 47 to col. 8, l. 20, col. 13, ll. 18-44, claim 1). The output of said single scan chain observable at an I/O pad of said integrated circuit is inherently there because in order to scan in fuse data into the fuse box 206 a standard TAP interface must be present, therefore facilitating scanning in and observing the results in the form of scanning out.

Claim 5:

Shubat teaches said means for preventing includes a shift register (**registers 208A through 208D, Fig. 3A, col. 8, ll. 6-20**) for reading out the state of said fuses for passing the state of said fuses to a control circuit (**logic block 701A and logic block 701B, col. 11, ll. 3-43**), said control circuit adapted to disable failing macro-circuits directly or adapted to disable failing macro-circuits under the direction of an electronic system said integrated circuit is electrically connected to. (Abstract, Col. 2, l. 46 to col. 3, l. 37, col. 7, l. 47 to col. 8, l. 20, col. 13, ll. 18-44, claim 1).

Claim 6:

Shubat teaches one or more repairable circuits (redundant portion 13), said fuse bank further including additional fuses (**Fuses Box 206, Fig. 3A**) for storing repair data

for said repairable circuits; and an additional shift register serially connected to said shift register (**registers 208A through 208D, Fig. 3A**), said additional shift register for reading out the state of said additional fuses and for passing the state of said fuses to a repair circuit, said repair circuit adapted to replace failing portions of said repairable circuits with redundant good circuits. (Abstract, Col. 2, l. 46 to col. 3, l. 37, col. 7, l. 47 to col. 8, l. 20, col. 13, ll. 18-44, claim 1).

Claim 9:

Shubat teaches said fuses are selected from the group consisting of laser blow fuses, electrical blow fuses or electrical blow antifuses (**although laser fuses have been exemplified in the present patent application, the teachings herein are applicable to a variety of fuses such as, for example, non-volatile memory fuses, electrical fuses, et cetera, col. 17, ll. 6-10**).

Claim 10:

Shubat teaches providing an integrated circuit (**202, Fig. 3A**) having a multiplicity of macro-circuits (**memory instances 204A – 204D, Fig. 3A**) arranged in one or more groups, each macro circuit of the same group having the same function, and a fuse bank containing fuses (**Fuses Box 206, Fig. 3A**), isolating said macro-circuits from other circuits of said integrated circuit, testing each macro-circuit prior to a fuse programming operation (**By scanning appropriate location information into the redundancy scan flip-flops 304 before the fuse data is entered (i.e., prior to laser-blowing the fuses) and scanning that information out on a field-by-field basis, redundant wordlines or bitlines in individual memory instances may be pre-tested**

easily), programming said fuses in said fuse bank in order to store data indicating at least which macro-circuits failed said testing step and preventing utilization of each failing macro-circuit during operation (**registers 208A through 208D, Fig. 3A**) of said integrated circuit based on the data stored in said fuse bank. (Abstract, Col. 2, l. 46 to col. 3, l. 37, col. 7, l. 47 to col. 8, l. 20, col. 9, ll. 56-65 col. 10, l. 49 to col. 11, l. 2, claim 22).

Claim 11:

Shubat teaches said integrated circuit further includes first scan chains (**register 208A**) coupling said other circuits, second scan chains coupled to said macro-circuits (**register 208B**) and isolation circuits (**fuse box 206 contains a plurality of fuses 302**) coupled to third scan chains (**the fuse box 206 is also provided with a plurality of redundancy scan flip-flops 304, col. 9, ll. 29-36**), said isolation circuits coupled between said other circuits and said macro-circuits. Shubat also teaches the steps of coupling said first, second and third scan chains into a first configuration to achieve isolation of said other circuits from said macro-circuits and coupling said first, second and third scan chains into a second configuration to achieve isolation of said macro-circuits from each other and from said other circuits (**The daisy-chain arrangement among the fuses and redundancy scan flip-flops allows individual fuse contents to be read out by easy scanning, col. 16, ll. 52-55**). (Abstract, Col. 2, l. 46 to col. 3, l. 37, col. 7, l. 47 to col. 8, l. 20, col. 9, ll. 56-65 col. 10, l. 49 to col. 11, l. 2, claim 22).

Claim 12:

Shubat teaches said testing includes applying sequentially one or more test patterns to each macro-circuit in each group macro-circuits and determining failing macro-circuits one group at a time (**A redundant memory area of the memory circuit is pre-tested to verify its functionality. The main memory area is tested thereafter to determine faulty locations, col. 3, ll. 5-10, col. 9, ll. 29-66**). (Abstract, Col. 2, l. 46 to col. 3, l. 37, col. 7, l. 47 to col. 8, l. 20, col. 9, ll. 56-65 col. 10, l. 49 to col. 11, l. 2, claim 22).

Claim 14:

Shubat teaches writing data indicating at least which macro-circuits failed to a fuse blow file in a tester performing said testing; and wherein said programming is performed based on data in said fuse blow file in that the OV_RSCIN signal 306 is provided for entering arbitrary address or location information in an override mode into the redundancy scan flip-flops 304 provided in the fuse box 206. In the override mode the contents of the fuses are bypassed. Shubat also teaches by scanning appropriate location information into the redundancy scan flip-flops 304 before the fuse data is entered (i.e., prior to laser-blowing the fuses) and scanning that information out on a field-by-field basis, redundant wordlines or bitlines in individual memory instances may be pre-tested easily. Shubat further teaches the fuses are blown based on this information. (col. 9, ll. 29-66). The claimed "a fuse blow file in a tester" is inherently present in Shubat because the scanned in location information and scanning out the failed information can not be performed without these features. (Abstract, Col. 2, l. 46 to

col. 3, l. 37, col. 7, l. 47 to col. 8, l. 20, col. 9, ll. 56-65 col. 10, l. 49 to col. 11, l. 2, claim 22).

Claim 19:

Shubat teaches the step of preventing includes disabling failing macro-circuits under the direction of an electronic system said integrated circuit is electrically connected to in that the OV_RSCIN signal 306 is provided for entering arbitrary address or location information in an override mode into the redundancy scan flip-flops 304 provided in the fuse box 206. In the override mode the contents of the fuses are bypassed. Shubat also teaches by scanning appropriate location information into the redundancy scan flip-flops 304 before the fuse data is entered (i.e., prior to laser-blowing the fuses) and scanning that information out on a field-by-field basis, redundant wordlines or bitlines in individual memory instances may be pre-tested easily. Shubat further teaches the fuses are blown based on this information. (col. 9, ll. 29-66). The claimed "a fuse blow file in a tester" is inherently present in Shubat because the scanned in location information and scanning out the failed information can not be performed without these features. (Abstract, Col. 2, l. 46 to col. 3, l. 37, col. 7, l. 47 to col. 8, l. 20, col. 9, ll. 56-65 col. 10, l. 49 to col. 11, l. 2, claim 22).

Claim 20:

Shubat teaches said fuses are selected from the group consisting of laser blow fuses, electrical blow fuses or electrical blow antifuses (**although laser fuses have been exemplified in the present patent application, the teachings herein are**

applicable to a variety of fuses such as, for example, non-volatile memory fuses, electrical fuses, et cetera, col. 17, ll. 6-10).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shubat et al. (US-6363020), hereinafter Shubat.

Claim 15:

Shubat teaches performing a post fuse blow test, said post fuse blow test including in the order recited: masking each failing macro-circuit based on the data in said fuse bank; applying sequentially one or more test patterns to each macro-circuit in each group of macro-circuits and determining failing macro-circuits one group at a time. (Abstract, Col. 2, l. 46 to col. 3, l. 37, col. 7, l. 47 to col. 8, l. 20, col. 9, ll. 56-65 col. 10, l. 49 to col. 11, l. 2, claim 22).

The limitation "terminating post fuse blow test upon any macro-circuit failing" has not been claimed by the applicant as having a patentable distinction or feature that would distinguish the device from other devices. Instead, this "terminating post fuse blow test" appears to be in the realm of design requirements in the practice of sound engineering principles, to terminate a test "upon any macro-circuit failing", rather than a

unique circuit feature that would be patentable, and therefore represents a prima facie case of obviousness. Since this is an obvious design choice to one skilled in the art, the claim is rejected.

Applicants can rebut a prima facie case of obviousness by showing the criticality of the claimed arrangement. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP § 716.02 - § 716.02(g) for a discussion of criticality and unexpected results.

Claim 16:

Shubat teaches after performing said post fuse test, packaging said integrated circuit into a module; and performing a module test, said module test including in the order recited: masking each failing macro-circuit based on the data in said fuse bank; applying sequentially one or more test patterns to each macro-circuit in each group of macro-circuits and determining failing macro-circuits one group at a time. (Abstract, Col. 2, l. 46 to col. 3, l. 37, col. 7, l. 47 to col. 8, l. 20, col. 9, ll. 56-65 col. 10, l. 49 to col. 11, l. 2, claim 22).

The limitation "terminating post fuse blow test upon any macro-circuit failing" has not been claimed by the applicant as having a patentable distinction or feature that would distinguish the device from other devices. Instead, this "terminating post fuse

blow test" appears to be in the realm of design requirements in the practice of sound engineering principles, to terminate a test "upon any macro-circuit failing", rather than a unique circuit feature that would be patentable, and therefore represents a prima facie case of obviousness. Since this is an obvious design choice to one skilled in the art, the claim is rejected.

Applicants can rebut a prima facie case of obviousness by showing the criticality of the claimed arrangement. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP § 716.02 - § 716.02(g) for a discussion of criticality and unexpected results.

9. Claims 4, 7, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shubat et al. (US-6363020), hereinafter Shubat in view of Seitoh (US-6829181), hereinafter Seitoh.

Claims 4, 7, 17 and 18:

Shubat does not explicitly teach "said macro-circuits are microprocessors and said means for preventing generates a busy signal for each macro-circuit that failed said test" (these limitations are included in claim 17 and 18). However, Shubat does teach advantages of his invention are more particularly emphasized in the context of memory compilers used for the design of embedded memories, e.g., SOC devices, custom-

specific ICs, et cetera. Accordingly, those of ordinary skill in the art should realize upon reference hereto that Shubat's invention may preferably be embodied in any suitable IP form. Seitoh teaches in an analogous art a failure address storage memory 120 which comprises an SRAM or the like and stores therein non-failure/failure information detected by a test, and a BIST (Build In Self Test) (a built-in test circuit as per claim 4) control circuit 160 which controls test operations in the chip. Seitoh also teaches the flash memory is configured so as to output a ready/busy signal R/B indicative of whether accessing is allowed from outside, to the outside according to predetermined bits of the status register which reflects the internal state of the memory. (Col. 17, ll. 16-39). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Shubat's memory instances 204A-D and registers 208A-D to use Seitoh's system of testing the embedded memory (FLASH) of a processor to include the busy signal R/B. The artisan would be motivated to do so because it would enable Shubat to indicate the predetermined bits of the status register which reflects the internal state of the memory(i.e. the pass/fail information stored in the redundant registers 208A-D).

10. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shubat et al. (US-6363020), hereinafter Shubat in view of Di Ronza et al. (US-6757204), hereinafter Di Ronza.

Claim 8:

Shubat does not explicitly teach "said fuse bank stores compressed data and further including means for decompressing said compressed data". However, Shubat does teach a control circuit (**logic block 701A and logic block 701B, col. 11, ll. 3-43**) as per the rejection of claim 5. Di Ronza teaches in an analogous art **a fuse box controller** that compresses/decompresses data outputted to the integrated circuit modules and/or compresses data inputted from the integrated circuit modules into the fuse box. (Col. 6, ll. 16-56). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Shubat's control circuit (**logic block 701A and logic block 701B**) to include Di Ronza's **fuse box controller**. The artisan would be motivated to do so because in using compressed/decompressed data Shubat will be able to use less fuse elements within the centralized fuse box 206 saving area and increasing shifting times to the redundant registers 208A-D.

11. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shubat et al. (US-6363020), hereinafter Shubat in view of DeBrosse et al. (US-5610867), hereinafter DeBrosse.

Claim 13:

Shubat does not explicitly teach "keeping a count of failing macro-circuits during testing and terminating testing when the number of failing macro-circuits exceeds a predetermined number". DeBrosse teaches in an analogous art in the testing of a DRAM if the number of failures exceed a predetermined margin (box 264, Fig. 6) the test is terminated (box 266, Fig. 6). It would have been obvious to one of ordinary skill in

the art at the time the invention was made to modify Shubat's testing method to check for failures that exceed a predetermined margin as in DeBrosse's method. The artisan would be motivated to do so because it would enable Shubat to save testing time when a particular memory is found to exceed that limit.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Cowan et al. (US-6505324) teaches all the aspects of the claimed invention, including using fuses in macros.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000

John J. Tabone, Jr. 3/22/07
Examiner
Art Unit 2138